What is claimed is:

1. A computer system comprising:

a non volatile memory in which is stored a firmware error handling routine for handling errors; and

at least one processor wherein each of the at least one processors detects errors and executes the firmware error handling routine on detecting an error to handle the error and wherein the firmware error handling routine logs error information to a log.

2. The computer system of claim 1, wherein the error handling routine collects state information, saves the state information to the log, analyzes the error and attempts to correct the error.

3. The computer system of claim 1 wherein the firmware error handling routine analyzes the error and determines a severity of the error and handles a plurality of detected errors in order of the severity of the error.

4. The computer system of claim 2 further comprising:

a system memory in which is stored an operating error handling routine for handling errors; and

wherein the at least one processor executes the operating system error handling routine on failure to correct the error by the firmware error handling routine.

5. The computer system of claim 4, wherein the operating error handling routine attempts to correct the error by terminating processes affected by the error.

6. The computer system of claim 5, wherein the operating error handling routine reboots the system on failure to correct the error.

7. A computer system comprising:

a non volatile memory in which is stored a processor abstraction layer error handling routine and a system abstraction layer error handling routine; and

a processor coupled to the non volatile memory for executing the processor abstraction layer error handling routine and the system abstraction layer error handling routine on detecting an error.

8. The computer system of claim 7 further comprising:

platform hardware coupled to the processor, wherein the processor detects errors in the platform hardware as errors.

9. The computer system of claim 7, wherein error handling is cooperatively performed by the processor, the processor abstraction layer and the system abstraction layer.

10. The computer system of claim 9, wherein the system abstraction layer error handling routine analyzes the error and the state information, obtains additional state information by utilizing processor abstraction layer procedures, determines a severity of the error, creates a log containing the state information, and attempts to correct the error on processor abstraction layer being unable to correct the error.

11. A computer system comprising:

a plurality of systems comprising:

a non volatile memory in which is stored a first error handling routine and a second error handling routine; and

a processor coupled to the non volatile memory to execute the first error handling routine and the second error handling routine and to generate an error log on detecting an error.

12. A system for cooperative error handling comprising:

a memory in which is stored a first error handling routine for correcting errors and a second error handling routine for correcting errors; and

a detecting processor coupled to the non volatile memory to detect errors, to execute the first error handling routine on detecting an error, to execute the second error handling routine on failure of the first error handling routine to correct the error.

13. The system of claim 12, further comprising a system memory coupled to the detecting processor in which is a third error handling routine wherein the detecting processor executes the third error handling routine on failure of the first and second error handling routines to correct the error.

14. A system comprising:

a processor;

a system memory; and

a non-volatile memory in which is stored:

a first error handling routine executed on an error to access state information, store the state information to a log and to attempt to correct the.

15. The system of claim 14, wherein the non-volatile memory further comprises a second error handling routine branched to on completion of the first error handling routine, wherein the second error handing routine stores a status of the error and the state information to the log and attempts to correct the error.

16. The system of claim 15, wherein the system memory further comprises a third error handling routine executed by the processor on failure of the second error handling routine to correct the error, wherein the third error routine accesses the log and attempts to correct the error by terminating affected processes and wherein the first error handling routine is a processor abstraction layer error handling routine, the second error

handling routine is a system abstraction layer error handling routine and the third error handling routine is an operating system error handling routine.

17. The system of claim 16, wherein the third error handling routine causes the system to reboot on failure to correct the error.

18. A method for cooperative error handling in a computer system comprising:

detecting an error by a detecting processor;

executing error handling code of a first layer of software, by the detecting processor, to perform the following:

saving state information;

attempting to correct the error;

on failure to correct the error, executing error handling code of a second layer of software by the detecting processor to perform the following:

determining severity of error by analyzing state information and the error received from the first layer;

saving additional state information; and

halting the computer system if necessary; and

on failure to correct the error by the second layer of software, executing error handling code of an operating system by the detecting processor to perform the following:

checking state information and the error to see if processing can continue;

halting the computer system if processing unless processing can continue; and

attempting to correct the error.

19. A method for handling errors in a system comprising:

detecting an error;

determining if the error is global or local;

on the error being global, signaling other processors of the error and allowing one processor to control error handling;

determining if the error is unrecoverable;

on the error being unrecoverable, halting the system;

correcting the error.

20. The method of claim 19, further comprising:

interrupting affected processes; and

resuming the affected processes after correcting the error.

21. The method of claim 19, further comprising:

saving state information; and

determining a severity of the error.

22. A method comprising:

detecting an error;

sending a signal to a processor abstraction layer, a system abstraction layer, and an operating system of the error;

interrupting processing if necessary;

attempting to correct the error by the processor abstraction layer and informing the system abstraction layer of success or failure in correcting the error;

upon success by the processor abstraction layer, informing operating system of the correction;

upon failure by the processor abstraction layer, attempting to correct the error by the system abstraction layer and informing the operating system of success or failure;

upon failure by the system abstraction layer, attempting to correct the error by the operating system; and

upon failure by the operating system, initiating a system reboot.

23. The method of claim 22, further comprising determining a severity of the error and halting system on certain errors.

24. A computer readable medium containing computer instructions for instructing a processor to perform a method for cooperatively handling errors comprising:

attempting to correct an error by a detecting processor;

on failure, executing firmware code to correct the error; and

on failure, executing operating system code to correct the error.

25. The computer readable medium containing computer instructions for instructing a processor to perform a method for cooperatively handling errors, further comprising:

on the operating system being a legacy operating system, sending compatible instructions to the operating system.